

# CURRICULUM VITAE



PRIYABRAT GARANAYAK

Assistant Professor

Department of Electronics and Communication Engineering

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**Research Interests:** Harmonic parameter estimation, design of active and hybrid filters, unified power quality conditioner (UPQC), series-parallel uninterruptible power supply (SP-UPS), renewable energy systems, signal processing application in power system.

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## **1. Personal Profile**

**Father's Name:** Mr. Rabindra Kumar Garanayak

**Mother's Name:** Mrs. Sasmita Garanayak

**Date of Birth:** 04<sup>th</sup> October 1987

**Marital Status:** Single

**Nationality:** Indian

**Religion:** Hindu

**Category:** General

**Gender:** Male

**Language Known:** Odia, Hindi and English

**Corresponding Address:** Department of Electronics and Communication Engineering,

Indian Institute of Information Technology Pune,

Sadumbare, Talegaon, Pune, Maharashtra, Pin 412109

**Permanent Address:** Kendriya Vidyalaya Road, Banamali Prasad,

Dhenkanal 759001, Odisha, India

## 2. Academic Qualifications

Degree Obtained	Discipline	University	School/Institute	Year of Passing	GPA
Ph. D.*	Electrical Engineering	National Institute of Technology Meghalaya, Shillong	National Institute of Technology Meghalaya, Shillong, Meghalaya	2016	8.67/10
M. Tech**	VLSI and Embedded System Design	Biju Patnaik University of Technology, Odisha	Centre for Microelectronic, Rourkela, Odisha	2011	8.22/10
B. Tech	Electronics Telecommunication Engineering	Biju Patnaik University of Technology, Odisha	Synergy Institute of Engineering and Technology Dhenkanal, Odisha	2009	7.66/10
12 <sup>th</sup>	Science	Council of Higher Secondary Education, Orissa	Dhenkanal Junior College, Dhenkanal, odisha	2005	57.7%
10 <sup>th</sup>	General	Board of Secondary Education, Orissa	Khajuriakata High School, Dhenkanal, Odisha	2003	84.5%

\* *Thesis Title:* Power Quality Assessment and its Enhancement in a Distribution Power System Network

*Name of Supervisor:* Dr. Gayadhar Panda (Associate Professor, NIT Meghalaya)

\*\* *Thesis Title:* Design and Implementation of Adaptive Noise Canceller

*Name of Supervisors:* Dr. Jitendra Kumar Das (Associate Professor, KIIT University) and Tapas Kumar Patra (Assistant Professor, CET Bhubaneswar)

## 3. Research Experiences

Name of the Organization	Position Held	Period From	Period To	Nature of Work
Indian Institute of Technology Delhi, New Delhi	Project Associate	Aug 2016	July 2017	Research work
National Institute of Technology Meghalaya, Shillong	Junior Research Fellow	Sep 2013	Jan 2014	Research work and B. Tech Laboratories Handle

## 4. Teaching Experiences

Name of the Organization	Position Held	Period From	Period To	Nature of Work
Indira Gandhi Institute of Technology, Sarang, Odisha	Lecturer	Feb 2013	Aug 2013	B. Tech Classes and Laboratories Handle
International Institute of Engineering & Technology, Bhubaneswar, Odisha	Guest Lecturer	Sept 2010	Dec 2012	B. Tech Classes and Laboratories Handle

## 5. Publications

### Journals:

- (a) **P. Garanayak** and G. Panda, “Fast and accurate measurement of harmonic parameters employing hybrid adaptive linear neural network and filtered-x least mean square algorithm”, *IET Generation, Transmission & Distribution*, vol. 10, no. 2, pp. 421–436, Feb. 2016. (SCI Journal, 2016 Impact Factor 2.213)
- (b) **P. Garanayak**, G. Panda, and P. K. Ray, “Harmonic estimation using RLS algorithm and elimination with improved current control technique based SAPF in a distribution network”, *International Journal of Electrical Power & Energy Systems (Elsevier)*, vol. 73, pp. 209–217, Dec. 2015. (SCI Expanded Journal, 2016 Impact Factor 3.289)
- (c) **P. Garanayak** and G. Panda, “Harmonic elimination and reactive power compensation by novel control algorithm based active power filter”, *Journal of Power Electronics*, vol. 15, no. 6, pp. 1619–1627, Nov. 2015. (SCI Expanded Journal, 2016 Impact Factor 1.047)
- (d) **P. Garanayak** and G. Panda, “An ADALINE with Nonlinear Weight Updating Rule Employed for Harmonic Identification and Power Quality Monitoring”, *Transactions of the Institute of Measurement and Control (SAGE)*, Mar. 2017, DOI: 10.1177/0142331217695402. (SCI Expanded Journal, 2016 Impact Factor 1.049)

### Conferences & Seminar Presentation:

- (a) **P. Garanayak**, G. Panda and P. K. Ray, “Power System Harmonic Parameters Estimation using ADALINE-VLLMS Algorithm”, *IEEE International Conference on Energy, Power and Environment: Towards Sustainable Growth (ICEPE 2015)*, pp. 1–6, NIT Meghalaya, Jun. 2015.
- (b) **P. Garanayak** and G. Panda, “FPGA Based Shunt Hybrid Active Power Filter for Harmonic Mitigation”, *5<sup>th</sup> International Exhibition & Conference, New Technologies in Transmission, Distribution, Smart Grid & Communication (GRIDTECH-2015)*, pp. 560–567, New Delhi, Apr. 2015.
- (c) **P. Garanayak** and G. Panda, “A novel current control technique to enhance dynamic performance of shunt active power filter”, *All India Seminar on Recent Advances in Power, Energy and control (RAPEC-2013)*, NIT Rourkela, Nov. 2013.
- (d) **P. Garanayak** and Gayadhar Panda, “Review on power quality improvement in a distribution network using active power filters”, *National Seminar on Development of Smart Grid in India*, NEHU Shillong, Nov. 2014.

## 6. Short-term Courses/Workshops Attended

Name of the Course	Period From	Period To	Institute/Industry	Sponsored by
Short-term course on Renewable Energy Conversion Technology (RECT-2014)	23 <sup>rd</sup> Sep 2014	24 <sup>th</sup> Sep 2014	North-Eastern Hill University, Shillong	Power Electronics Group CDAC
National Workshop on Recent Advances in Power, Control & Energy (RAPCE 2014)	25 <sup>th</sup> Apr 2014	26 <sup>th</sup> Apr 2014	National Institute of Technology Meghalaya, Shillong	Power Grid and NEPCO
Short-term course on Power Electronics System & Applications (PESA 2014)	4 <sup>th</sup> Apr 2014	6 <sup>th</sup> Apr 2014	National Institute of Technology Rourkela, Odisha	NaMPET
Refresher Course on Power Electronics, Drives and Power Quality Issues	23 <sup>rd</sup> Dec 2013	27 <sup>th</sup> Dec 2013	National Institute of Technology Rourkela, Odisha	-

## 7. Competitive Exams

- Graduate Aptitude Test in Engineering (GATE) - 2011, India (National Level), Discipline: EC, Percentile: 92%
- Post Graduate Admission Test (PGAT) - 2009, Odisha, India (National Level), Discipline: EC, Rank: 50

## 8. Sponsored Projects

Sponsoring Agency	Title of the Project	Period	Amount	Status
DST-SERB	Proposal of a New Generation Power Converter for Harmonic Elimination, Reactive Power Compensation and Load Balancing in Medium Voltage Applications	2 Years	19,20,000/-	Under Review (File Number PDF/2017/375/ES)

## 9. Achievements and Awards

- Awarded best position, in Odisha State Talent Scholarship Examination conducted by World Health and Education Service.
- Awarded 3<sup>rd</sup> position in Essay competition at High School level conducted by Board of Secondary Education, Odisha.

## **10. Extension Works/ Community Services**

- (a) Reviewer of reputed journals (IEEE Transaction on Industrial Electronics, IEEE Transaction on Circuit and System I, Electric Power Components and Systems, IET Generation, Transmission & Distribution).
- (b) Reviewed papers in conference (ICEPE-2015).

## **11. Hobbies**

- (a) Reading “Electronics for You” Magazine.
- (b) Painting Cartoons.

## **12. Membership of Professional Bodies**

- (a) IEEE Student Member
- (b) IET Student Member

## **12. Referees**

- (a) **Dr. Gayadhar Panda** (Associate Professor)  
Department of Electrical Engineering,  
National Institute of Technology Meghalaya, India
- (b) **Dr. Sukumar Mishra** (Professor)  
Department of Electrical Engineering,  
Indian Institute of Technology Delhi, India
- (c) **Dr. Pravat Kumar Ray** (Assistant Professor)  
Department of Electrical Engineering,  
National Institute of Technology Rourkela, India
- (d) **Dr. Anup Dandapat** (Associate Professor, Dean Academic)  
Department of Electronics & Communication Engineering,  
National Institute of Technology Meghalaya, India

### **Declaration**

I hereby declare that all information furnished above is true to the best of my knowledge.